F 9328 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2011

Fourth Semester

Branch : Computer Science and Engineering

COMPUTER ORGANIZATION (R)

(2002 Admissions onwards—Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. With a neat diagram, explain the data path used for fetching instruction and incrementing the program counter.
2. Explain the basic control signals to be generated by a processor for memory and I/O operations.
3. Explain signed multiplication.
4. Describe addition and subtraction done in a computer system with appropriate examples.
5. Explain the memory transfer operation using micro instructions.
6. Describe how a micro instruction is executed in horizontal approach.
7. Differentiate between compulsory miss and capacity miss in memory.
8. Explain with a neat diagram, a 4-way set associative Cache.
9. Explain the working of a mouse.
10. Explain interrupt driven I/O techniques.

(10 × 4 = 40 marks)

Part B

Answer any **one** *full question from each module*
Each question carries 12 *marks.*

Module 1

11. Describe the various operation cycles involved in the running of a program.

Or

12. What are the different bus structures ? Explain under what circumstances, we may go for multiplexing buses.

Module 2

13. Design an Accumulator circuit that is used to perform the arithmetic and logic operations on datas of 4 bit. Illustrate with one stage of ALU.

Or

14. Clearly explain various techniques used by high performance processors to reduce the time needed for multiplication.

Module 3

15. Explain the implementation of microcode controller used for microprogram execution.

Or

16. (a) What are the functions and uses of PLAs ?

(b) Explain bit-slice microinstruction format and its processor.

Module 4

17. Give the features of Cache memory. What is the role of compiler optimization technique in reducing the Cache misses ?

Or

18. Explain the address translation from virtual address to physical address in a paged segmented memory system. What are the additional address bits required in such a translation ? How does a TLB improves the speed of address translation ?

Module 5

19. Specify the characteristics of (i) parallel bus standard IEEE 488, and (ii) serial communication standard-current loop, RS 232 C, with suitable illustration for each case.

Or

20. Specify the characteristics of an IO processor :

(a) Its interactions with CPU.

(b) Sequence of actions for executing an IO program.

(c) Sequence of actions of CPU initiated IO data transfer.

(d) Sequence of actions for device initiated IO data transfer.

(5 × 12 = 60 marks)