F 3470 (Pages : 3) Reg. No...................................

Name......................................

B.TECH. DEGREE EXAMINATION, NOVEMBER 2010

Third Semester

Branch : Computer Science and Engineering

LOGIC SYSTEM DESIGN (R)

(Regular/Improvement/Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 marks.

1. Perform the following subtractions using 2's complement method :

   (a) 01100 – 00011.

   (b) 0011.1001 – 0001.111.

2. What are haming codes ? Explain their applications.

3. For the logic equation $f = \text{ABC} + \text{B}\bar{\text{C}}\text{D} + \bar{\text{A}}\text{BC}$, construct the truth table and simplify using K-map.

4. Find the dual of the following functions :

   (a) $f_1 = xyz + x'y\,z'$.

   (b) $f_2 = (x + y')z + x'yz'$.

5. Give the excitation tables of JK and D flip-flops.

6. Draw a logic diagram of a clocked D flip-flop using AND and NOR gates.

7. Implement a full adder using two half adders and draw the diagram.

8. Compare and contrast between serial and parallel adders.

9. Draw and explain the application of the ring counter, with its timing diagram.

10. Explain the working of a 3-bit serial-in, serial-out shift register, with logic diagram.

(10 × 4 = 40 marks)

Turn over

Part B

Answer **either** *Section (a)* **or** *(b) from each Module.*
Each full question carries 12 *marks.*

MODULE 1

11. (a) (i) Encode the following decimal numbers to BCD code :

(1) 640 ; (2) 372.98 ; (3) 20.301.

(6 marks)

(ii) Encode the above numbers to Gray codes. (6 marks)

Or

(b) (i) Convert the following decimal numbers into hexadecimal numbers :

(1) 9527 ; (2) 675.231 ; (3) 0.728.

(6 marks)

(ii) Explain error detection and correction codes with the help of suitable examples.

(6 marks)

MODULE 2

12. (a) Minimize the four variable function using K-map and realise the minimal SOP and POS forms : $f = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$.

(12 marks)

Or

(b) A stair-case light is controlled by two switches, one at the top of the stairs and another at the bottom of the stairs

(i) make a truth table for this system.

(ii) write the logic equation in SOP form.

(iii) realise the circuit using AND-OR-gates ;

(iv) realise the circuit using only NOR gates.

(12 marks)

MODULE 3

13. (a) Design a mod-6 synchronous counter using clocked JK flip-flop, from the fundamentals. Draw the circuit and timing waveforms.

(12 marks)

Or

(b) (i) Draw the circuit diagram of a clocked SR flip-flop using only NAND gates and explain its truth table.

(8 marks)

(ii) What are the merits and demerits of master slave JK flip-flop ? Explain. (4 marks)

MODULE 4

14. (a) Design a one-digit BCD adder and draw its circuit diagram.

Or

(b) With neat circuit diagrams, explain the principles of (i) carry look ahead adder ; (ii) carry save adder and compare their performances.

(12 marks)

MODULE 5

15. (a) Design a 4-stage ring counter. What is the need of self correction circuit ? Give a self correction circuit for the above counter.

Or

(b) Draw the logic diagram for a four-bit parallel input/parallel output register. Indicate inputs, outputs and a negative edge-triggered clock and describe its working.

(12 marks)

[5 × 12 = 60 marks]