G 6776 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, APRIL 2011

Third Semester

Branch : Computer Science and Engineering

LOGIC SYSTEM DESIGN (R)

(2002 admission onwards—Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. (a) Add 17_{10} and 95_{10} in binary ; (b) substract 11100101_2 from 11110111_2 using 1's complement method.
2. What is Gray code ? What is its use ? Convert the binary number 10110 to Gray code.
3. Simplify $f(a,b,c,d) = \sum m\,(0,1,2,4,5,6,8,14)$ using K-map.
4. Prove the universality of NAND and NOR gates.
5. With truth tables and logic circuit, explain the working of SR and JK flip flops.
6. Explain a mode-7 ripple upcounter.
7. Implement half adder using basic gates and show the implementation of full adder using half adders.
8. Describe the principle of a carry save adder.
9. What is a ring counter ? What are its applications ?
10. Describe how shift registers can be used to perform binary arithmetic operations.

(10 × 4 = 40 marks)

Part B

Answer any **one** *full question from each module.*
Each full question carries 12 *marks.*

Module 1

11. (a) (i) Convert the following hexadecimal numbers to the binary :
    (1) 671.176 (2) IF1.90 A (3) 20D.CA1. (6 marks)
    (ii) Explain ASCII and EBCDIC codes. (6 marks)

Or

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(b) (i) Perform the following subtractions using 2's complement method.

(1) 01000 – 01001 ; (2) 01100 – 00011 ; (3) 0011.1001 – 0001.1110.

(ii) Encode the following decimal numbers into BCD codes :

(1) 327.09 ; (2) 200.009 ; (3) 110.901. (6 marks)

Module 2

12. (a) Minimise using K-map and draw the logical minimal circuit using basic logic gates :

(i) $f_1 = \Sigma m\,(2,8,9,10-12) + \phi\,\Sigma\,(3,6,13-15)$. (6 marks)

(ii) $f_2 = (a+\bar{b})\,(a+c+d)\,(\bar{a}+\bar{b}+\bar{d})\,(a+\bar{c}+d)$. (6 marks)

Or

(b) Find all the prime implicants of the function using Quine McCluskey algorithm

$f = \pi M\,(0,2,3,4,5,12,13) + dc\,(8,10)$.

Module 3

13. (a) Design a synchronous mod-9 counter using negative edge triggered JK flip-flop using excitation tables. Explain the working of the circuit using its timing diagram.

Or

(b) Design a seqeunce generator having the following repeated binary sequence using JK flip-flops :

$0 \rightarrow 1 \rightarrow 4 \rightarrow 6 \rightarrow 7 \rightarrow 5 \rightarrow 0$.

Module 4

14. (a) Draw the truth table of full substractor. Using K-maps, design the minimal logic, circuit using only NAND gates.

Or

(b) Draw the circuit of a 4-bit carry look ahead adder and explain its performance.

Module 5

15. (a) Draw circuit diagram of a 4-bit bidirectional shift register. Explain its working with timing diagram.

Or

(b) (i) With a neat circuit diagram and timing waveforms, describe the working of a 4-bit twisted ring counter. (8 marks)

(ii) Draw and explain the working of a 4-bit serial shift register. (4 marks)

[5 × 12 = 60 marks]