F 3165 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, DECEMBER 2012

Seventh Semester

Branch : Electronics and Communication Engineering / Applied Electronics and Instrumentation Engineering

VLSI TECHNOLOGY (LA)

(Regular/Supplementary/Mercy Chance)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. Compare ion implantation with diffusion.
2. Write the complementary error function used to describe the diffusion process and explain each term and its significance.
3. What is self-aligned polysilicon gate NMOS process? Explain.
4. Differentiate between trench isolation and silicon on insulator isolation.
5. What are the advantages of n-well CMOS technology?
6. Draw the stick diagram of a CMOS inverter.
7. Draw the layout diagram for two-input NOR gate.
8. Compare n-well CMOS and BiCMOS technologies.
9. Why alloyed contacts are preferred in MESFET fabrication? Explain.
10. Write a descriptory note on channelling effect.

(10 × 4 = 40 marks)

Part B

Answer any **one** *full question from each module.*
Each full question carries 12 *marks.*

MODULE I

11. Explain with neat diagrams, the different lithographic steps involved in selective diffusion over a wafer.

Or

Turn over

12. What is epitaxial growth? Discuss the different techniques used to grow epitaxial layer.

MODULE II

13. Explain in detail, with neat diagrams, the process of junction-isolated bipolar components in monolithic IC.

Or

14. With neat sketches, explain the *p*-well process for CMOS fabrication. Also give details of masks required at each step.

MODULE III

15. Explain with necessary sketches, the twin-tub CMOS process in detail. What is latch up and what are the remedies?

Or

16. Sketch and explain the different steps showing the fabrication of junction isolated BiCMOS integrated circuit process. Also comment on BiCMOS structure with multiple wells.

MODULE IV

17. Draw neat layout for:

    (i) 3 input AND gate. (6 marks)

    (ii) 2 input NOR gate. (6 marks)

Or

18. (a) Derive an expression for the dynamic power dissipation in a CMOS inverter. (6 marks)

    (b) What are λ-based design rules? Write the λ-rules for poly, diffusion layers, metals, and contacts. (6 marks)

MODULE V

19. Explain the doping process done in GaAs? What are its merits?

Or

20. Write neat diagrams describe the crystal structure of GaAs.

(5 × 12 = 60 marks)