F 3225 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, DECEMBER 2012

Seventh Semester

Branch : Electronics and Communication/Applied Electronics and Instrumentation/ Computer Science and Engineering/Information Technology

PRINCIPLES OF REAL TIME SYSTEMS (Elective I) (LART)

(Regular / Supplementary / Mercy Chance)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries **4** *marks.*

1. Explain a Aperiodic task class.
2. List and explain real time design issues.
3. Explain EDE algorithm.
4. Explain bin-packing algorithm.
5. What is a polled bus protocol? Explain.
6. Explain the different communication medias.
7. Determine the term "fault tolerance".
8. What is a master chain model? Explain.
9. Explain the characteristics of main memory database.
10. Explain the selection of a disk scheduling algorithm.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*

Each question carries **12** *marks.*

11 (a) Briefly explain the characteristics of a real time computer.

Or

(b) What is an embedded system? Explain the classification of embedded system.

Turn over

12. (a) Explain briefly a task control block and task status.

Or

(b) Compare and contrast utilization balancing algorithm and bin-packing algorithm.

13. (a) Explain different message sending topologies and its features.

Or

(b) What is synchronization? Explain how fault tolerent synchronization is done in hardware and in software.

14. (a) Explain how fault failure handling is done.

Or

(b) What is software error model? Explain in detail.

15. (a) Compare and contrast the Desired language characteristics and Realtime database characteristics.

Or

(b) Explain SSTF disk scheduling algorithm with examples.

(5 × 12 = 60 marks)