# MAHATMA GANDHI UNIVERSITY


## SCHEME AND SYLLABI

**FOR**

## M. Tech. DEGREE PROGRAMME

**IN**

# ELECTRONICS AND COMMUNICATION ENGINEERING

# WITH SPECIALIZATION IN

# VLSI & EMBEDDED SYSTEMS

**(2011ADMISSION ONWARDS)**

# SCHEME AND SYLLABI FOR M. Tech. DEGREE PROGRAMME IN ELECTRONICS AND COMMUNICATION ENGINEERING WITH SPECIALIZATION IN VLSI & EMBEDDED SYSTEMS

## SEMESTER - I

| Sl. No. | Course No. | Subject | Hrs / Week | | | Evaluation Scheme (Marks) | | | | | Credits (C) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | Sessional | | | ESE | Total | |
| | | | | | | TA | CT | Sub Total | | | |
| 1 | MEC VE 101 | Semiconductor Devices – Physics & Technology | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 2 | MEC VE 102 | Advanced Digital System Design | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 3 | MEC VE 103 | CMOS VLSI Design | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 4 | MEC VE 104 | Embedded System Design | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 5 | MEC VE 105 | Elective – I | 3 | 0 | 0 | 25 | 25 | 50 | 100 | 150 | 3 |
| 6 | MEC VE 106 | Elective – II | 3 | 0 | 0 | 25 | 25 | 50 | 100 | 150 | 3 |
| 7 | MEC VE 107 | VLSI Design Lab | 0 | 0 | 3 | 25 | 25 | 50 | 100 | 150 | 2 |
| 8 | MEC VE 108 | Seminar – I | 0 | 0 | 2 | 50 | 0 | 50 | 0 | 50 | 1 |
| **Total** | | | **18** | **4** | **5** | **225** | **175** | **400** | **700** | **1100** | **25** |

| Elective – I (MEC VE 105) | | Elective – II (MEC VE 106) | |
|---|---|---|---|
| MEC VE 105 - 1 | ASIC Design | MEC VE 106 - 1 | Processor architecture & Parallel processing |
| MEC VE 105 - 2 | High Speed Digital Design | MEC VE 106 - 2 | Modeling and Simulation of Electronic System |
| MEC VE 105 - 3 | Low Power VLSI Design | MEC VE 106 - 3 | System Design Using ARM |
| MEC VE 105 - 4 | Semiconductor memories | MEC VE 106 - 4 | Embedded Networks & Controllers |

**L** – Lecture, **T** – Tutorial, **P** – Practical

**TA** – Teacher's Assessment (Assignments, attendance, group discussion, Quiz, tutorials, seminars, etc.)

**CT** – Class Test (Minimum of two tests to be conducted by the Institute)

**ESE** – End Semester Examination to be conducted by the University

**Electives:** New Electives may be added by the department according to the needs of emerging fields of technology. The name of the elective and its syllabus should be submitted to the University before the course is offered.

# SEMESTER - II

| Sl. No. | Course No. | Subject | Hrs / Week | | | Evaluation Scheme (Marks) | | | | | Credits (C) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | Sessional | | | ESE | Total | |
| | | | | | | TA | CT | Sub Total | | | |
| 1 | MEC VE 201 | Analysis and Design of Analog Integrated Circuits | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 2 | MEC VE 202 | Advanced Embedded System Design | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 3 | MEC VE 203 | VLSI System Design | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 4 | MEC VE 204 | Real Time Operating Systems | 3 | 1 | 0 | 25 | 25 | 50 | 100 | 150 | 4 |
| 5 | MEC VE 205 | Elective – III | 3 | 0 | 0 | 25 | 25 | 50 | 100 | 150 | 3 |
| 6 | MEC VE 206 | Elective – IV | 3 | 0 | 0 | 25 | 25 | 50 | 100 | 150 | 3 |
| 7 | MEC VE 207 | Embedded System Lab | 0 | 0 | 3 | 25 | 25 | 50 | 100 | 150 | 2 |
| 8 | MEC VE 208 | Seminar-II | 0 | 0 | 2 | 50 | 0 | 50 | 0 | 50 | 1 |
| **Total** | | | **18** | **4** | **5** | **225** | **175** | **400** | **700** | **1100** | **25** |

| **Elective – III (MEC VE 205)** | | **Elective – IV (MEC VE 206)** | |
|---|---|---|---|
| MEC VE 205 - 1 | DSP System Design | MEC VE 206 - 1 | Analog & Mixed VLSI circuits |
| MEC VE 205 - 2 | MEMS & Micro system technology | MEC VE 206 - 2 | Testing of VLSI |
| MEC VE 205 - 3 | VLSI Signal Processing | MEC VE 206 - 3 | CAD for VLSI |
| MEC VE 205 - 4 | Hardware/Software Co Design | MEC VE 206 - 4 | Reconfigurable computing |

**L** – Lecture, **T** – Tutorial, **P** – Practical

**TA** – Teacher's Assessment (Assignments, attendance, group discussion, Quiz, tutorials, seminars, etc.)

**CT** – Class Test (Minimum of two tests to be conducted by the Institute)

**ESE** – End Semester Examination to be conducted by the University

**Electives:** New Electives may be added by the department according to the needs of emerging fields of technology. The name of the elective and its syllabus should be submitted to the University before the course is offered.

# SEMESTER - III

| Sl. No. | Course No. | Subject | Hrs / Week | | | Evaluation Scheme (Marks) | | | | | Credits (C) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | Sessional | | | ESE** (Oral) | Total | |
| | | | | | | TA* | CT | Sub Total | | | |
| 1 | MEC VE 301 | Industrial Training or Industrial Training and Mini Project | 0 | 0 | 20 | 50 | 0 | 50 | 100 | 150 | 10 |
| 2 | MEC VE 302 | Master's Thesis Phase - I | 0 | 0 | 10 | 100*** | 0 | 100 | 0 | 100 | 5 |
| **Total** | | | **0** | **0** | **30** | **150** | **0** | **150** | **100** | **250** | **15** |

* TA based on a Technical Report submitted together with presentation at the end of the Industrial Training **and** Mini Project

** Evaluation of the Industrial Training **and** Mini Project will be conducted at the end of the third semester by a panel of examiners, with at least one external examiner, constituted by the University.

*** The marks will be awarded by a panel of examiners constituted by the concerned institute

# SEMESTER - IV

| Sl. No. | Course No. | Subject | Hrs / Week | | | Evaluation Scheme (Marks) | | | | | Credits (C) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | Sessional | | | ESE** (Oral & Viva) | Total | |
| | | | | | | TA* | CT | Sub Total | | | |
| 1 | MEC VE 401 | Master's Thesis | 0 | 0 | 30 | 100 | 0 | 100 | 100 | 200 | 15 |
| 2 | MEC VE 402 | Master's Comprehensive Viva | | | | | | | 100 | 100 | |
| **Total** | | | | | **30** | **150** | **0** | **150** | **0** | **300** | **15** |
| **Grand Total of all Semesters** | | | | | | | | | | **2750** | **80** |

* 50% of the marks to be awarded by the Project Guide and the remaining 50% to be awarded by a panel of examiners, including the Project Guide, constituted by the Department

** Thesis evaluation and Viva-voce will be conducted at the end of the fourth semester by a panel of examiners, with at least one external examiner, constituted by the University.

**MEC VE 101 SEMICONDUCTOR DEVICES- PHYSICS & TECHNOLOGY**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module 1:**

Physics and Properties of Semiconductors - Crystal structure and energy band structure of semiconductors. Carrier concentration and transport, diffusion and drift; Basic semiconductor equations.

P-N Junction Diode – Theory of junction, minority carrier distribution and current components, forward bias, reverse bias, leakage current, breakdown.

**Module 2:**

Bipolar Transistor. Physics of operation, base transport factor, emitter efficiency, current gain ($\alpha$, $\beta$).

MOSFET - Basic device structures, NMOS, PMOS, operation physics. Parasitic bipolar transistor.

**Module 3:**

Oxidation technologies in VLSI and ULSI - Kinetics of Silicon dioxide growth both for thick, thin films- High k and low k dielectrics for ULSI- Solid State diffusion modeling and technology; Ion Implantation modeling, damage annealing.

**Module 4:**

Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI. CVD techniques for deposition of films; Etching- Evaporation and sputtering techniques- Plasma etching and RIE techniques.

**References:**


1. S.M. Sze, Physics of Semiconductor Devices, second edition, John Wiley, 1981.
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 2008.
3. S.M.Sze, Semiconductor Devices – Physics & Technology, second edition, Wiley India.
4. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 2008.
5. James Plummer, M. Deal and P.Griffin, Silicon VLSI Technology, Prentice Hall Electronics and VLSI series, 2nd Edition, 2009.

6. S.M.Sze (Ed), Modern Semiconductor Device Physics, John Wiley & Sons, 1998.
7. S.M. Sze and KK Ng, Physics of Semiconductor Devices, third edition, John Wiley, 2007.

**MEC VE 102 ADVANCED DIGITAL SYSTEM DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module -I Synchronous Sequential circuit Design analysis and Optimization**

Mealy and Moore model, State machine, Analysis of Synchronous sequential circuit, Design of Sequential Circuit – state equivalence, state reduction, state reduction of incompletely specified state table, State assignment technique. Design of Sequence Generator, Serial Binary Adders.

**Module- II Asynchronous Sequential Circuits**

Fundamental and Pulse mode Asynchronous sequential state machines, Analysis of Asynchronous Sequential state machine. Primitive Flow Table- Flow tables. State Assignment- Races and Cycles, Shared single row state assignment, shared multi row state assignment, one hot state assignment. Design of Asynchronous system with examples. Mixed operating mode Asynchronous circuits. Hazards- static, dynamic, essential. Design of vending machine controller.

**Module III Programmable Logic Memory**

Memory-ROM, PROM, EPROM, realization of sequential circuit using EPROM. Programmable Logic Devices (PLD)- PLA, PAL, Design using PAL. Gate Array Logic (GAL), design using GAL. EPLD- Altera EP600 EPLD. FPGA- Xilinx FPGA, System development tools for Xilinx FPGA, ACTEL FPGA.

**Module IV Digital System Design Using HDL**

Introduction to HDL - language elements, expressions, user defined primitives, types of modeling. Design using HDL- Flip flops, Counters, Shift registers, Multiplexers.

**References**

1. John M Yarbrough, “Digital Logic Applications and Design”, Thomson learning

2. A P Godse, “Digital System Design”, Technical publication
3. John F Wakerly, “Digital Design Principles and Practices”, PearsoN
4. Samuel C Lee, “Digital Circuits and Logic Design”, PHI
5. Michael D Ciletti, “Advanced Digital system Design with Verilog HDL”, PHI
6. Stephen Brown, “Fundamentals of Digital Logic with Verilog Design”, TMH
7. J Bhasker, “A verilog HDL Primer“, PHI
8. J Bhasker, “A VHDL Primer”, PHI

**MEC VE 103** **CMOS VLSI DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module 1:**

Brief review of NMOS, CMOS, and Bi-CMOS technologies - MOS Transistor theory CMOS Static logic design - Pseudo-NMOS - Full complementary CMOS - TG gate CMOS - Pass transistor Logic (PTL) families: DPTL, CPTL - DCVS logic - Realization using Binary decision diagrams.

**Module 2:**

CMOS Dynamic logic design - N-P Dynamic logic - Domino logic - NORA logic - TSPC logic - Multiple output Domino logic - Dynamic NORA dynamic logic circuits - Analysis of charge charging and noise problems in Dynamic logic circuits - FET scaling in dynamic logic circuits.

**Module 3:**

Bi-CMOS static logic design - Standard Bi-CMOS structures - Sub-3V Bi-CMOS structures - SOI CMOS static logic - Bi-CMOS Dynamic logic design - 1.5V Bi-CMOS dynamic logic circuit.

**Module 4: Timing Issues in Digital Circuits**

Technology scaling for sub-micron and deep sub-micron technologies - Design Issues and Solutions for Deep sub-micron sub-system design.

**Characterization and Performance estimation**: Design of VLSI Arithmetic Modules (adders, multipliers) - Area, power and delay estimates - Symbolic layout systems.

**References:**


1. Introduction to VLSI Circuits and Systems, J.P. Uyemura, Ed:Wiley India Edition, 2002.
2. CMOS VLSI Design Neil H E West, David Harris, Ayan Banerjee, Pearson Edu
3. CMOS Circuit Design, J.P. Uyemura, 1989
4. Sung Mo Kang and Yusuf Lebelci, “CMOS Digital integrated Circuits Analysis and Design”, Tata McGraw- Hill , New Delhi, 2003.

5. Jan M Rabaey and Anantha Chandrakasan, " Digital integrated Circuits- A Design Perspective" ,Prentice Hall, Second Edition, 2002.
6. Muller Richards, Kamins and Theodre "Device Electronics for Integrated Circuits" John Wiley, New York, 2003.

**MEC VE104** **EMBEDDED SYSTEM DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module 1:**

Introduction to Embedded Systems, Design challenges, optimization of design metrics. Processor Technology: General purpose Processor, Single-purpose processor, Application specific processor. IC and design Technology.

**Module 2: Single-purpose & General purpose processors**

Introduction to Single-purpose processors : Hardware **-** Combinational Logic, Sequential logic, Custom single-purpose processor design, RT-level custom single-purpose processor design, Optimizing custom single-purpose processors, Introduction to General-purpose processors: Software-Basic architecture, Operation, Programmer's view, Development environment, Application-specific instruction-set processors (ASIP's), Selecting a microprocessor, General-purpose processor design.

**Module 3: Peripherals and Interfacing**

Introduction to peripherals- Timers, Counters and WDTs, UART, PWM, LCD Controllers, Keypad Controllers, Stepper motor Controllers, A to D Converters, Real time clocks. Introduction to Interfacing- Communication Basics, Microprocessor interfacing , Arbitration, Multilevel Bus architectures, Advanced Communication principles, Serial-Parallel & Wireless.

**Module 4: R Introduction to Memory and Embedded System-Case Study**

Introduction to Memory, Common Memory types, Composing Memory, Memory Hierarchy and Cache, Advanced RAM. Case study of Digital Camera - Introduction, Requirement Specification, Design.

**References:**


1. Frank Frank Vahid and Tony Givargi, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2006
2. Wayne Wolf “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008.
3. Raj Kamal “Embedded Systems – Architecture, Programming and Design”, Tata McGraw Hill, 2nd Edition, 2008
4. Shibu K V “Introduction to Embedded Systems”, Tata McGraw Hill, 2010.

**MEC VE 105 - 1** **ASIC DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1:**

**Introduction to ASICs -** Types of ASICs – full custom ASIC – semi custom ASIC – standard cell based ASIC – gate array based ASIC – programmable ASIC – PLD – FPGA – Logical effort.

**Module 2:**

**Programmable ASICS, Programmable ASIC Logic cells -** Anti fuse- static RAM – EPROM and EEPROM technology, PREP benchmarks- Actel ACT-Xilinx LCA- Altera FLEX- Altera MAX – Architecture of FPGAs (Xilinx Spartan-3 – Altera Cyclone-3).

**Module 3**:

**Synchronous Design Using Programmable Devices-** EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 – Xilinx 3000. ).

**Module 4**:

**System Design Using Verilog HDL -** Verilog Description of combinational Circuits – arrays - Verilog operaters - Compilation and simulation of Verilog codes - Modelling using Verilog - Flip Flops – registers – counters - sequential machine - combinational logic circuits - Verilog codes – serial adders.

**References:**


1. M.J.S. Smith, “Application – specific integrated circuits” – Addison – Wesley Longman Inc. 1997.
2. John M Yarbrough “Digital Logic applications and Design”, Thomson Learning, 2001
3. Samir Palnitkar, “ Verilog HDL ”, Pearson Education, 1996.
4. Data sheet: Spartan-3 FPGA Family Advanced Configuration Architecture – Xilinx XAPP452 (v1.1) June 25, 2008
5. Cyclone III Device Hand book, Volume 1
6. Andrew Brown, - “VLSI circuits and systems in silicon”, Mc Graw Hill, 1991.

7. S.D. Brown, R.J. Francis, J.Rox, Z.G. Uranesic, “Field Programmable gate arrays”, Khuever academic publisher, 1992.
8. S.Y.Kung, H.J. Whilo House, T.Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
9. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning- 2004.

**MEC VE 105 - 2 HIGH SPEED DIGITAL DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module I**

High Speed Digital Design Fundamentals: Frequency and time, Time and distance, Lumped vs distributed, four kinds of reactance- ordinary capacitance and inductance, mutual capacitance and inductance, Relation of mutual capacitance and mutual inductance to cross talk.

High Speed properties of Logic gates: Power, Quicent vs active dissipation, Active power driving a capacitive load, Input power, Internal dissipation, drive circuit dissipation, Totem pole and open circuit speed, Sudden change in voltage and current.

Packaging of Digital Systems: Integrated circuit packages, Wire and cable, Connectors.

**Module II**

Measurement Techniques; Rise time and bandwidth of oscilloscope probes, self inductance of probe ground loop, Effects of probe load on a circuit, slow down of a system clock, observing cross talk, measuring operating margin.

Transmission Lines; Problems of point to point wiring, signal distortion, EMI, cross talk, ideal distortion less lossless transmission line, Electrical models of wires.

**Module III**

Transmission Lines at High frequency: Infinite uniform transmission line, Lossy transmission line, Low loss transmission line, RC transmission line, Skin effect, Mechanics of skin effect, Proximity effect, Dielectric loss, Effects of source and load impedance, Reflections of a transmission line, End termination, Source termination, Very short line

**Module IV**

Termination: end termination, Rise time, dc biasing, power dissipation, Source termination, Resistance value, Rise time, Power dissipation, Drive current, Middle terminators, Connectors – mutual, series and parasitic capacitance.

Power system: Stable voltage reference, Uniform voltage distribution, resistance and inductance distribution wiring, series resistance and lead inductance of a capacitance

Clock Distribution: schemes, Timing margin, Clock skew, delay adjustments, Clock jitter.

**Reference**


1. Howard Johnson, High-Speed Digital Design: A Handbook of Black Magic , Prentice Hall .
2. Dally W.S. & Poulton J.W., “Digital Systems Engineering”, Cambridge University Press.
3. Masakazu Shoji, “High Speed Digital Circuits”, Addison Wesley Publishing Company
4. Jan M, Rabaey, Digital Integrated Circuits: A Design perspective, Second Edition, 2003

**MEC VE 105 - 3** **LOW POWER VLSI DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1**: **Introduction, Physics of Power Dissipation in CMOS FET Devices**

Introduction – Need for VLSI, charging and discharging capacitance, short term current in CMOS circuit, CMOS leakage current, static current, basis principles of low power design, low power figure of merit. Physics of Power Dissipation in MOSFET Devices – power dissipation in CMOS, low power VLSI design limits.

Dynamic Power reduction technique - transition probability minimization, glitch reduction, supply voltage reduction, clock gating, multi-supply design, dynamic voltage and frequency scaling. Transition probability minimization: transition probabilities for some basic gates, inter-signal correlations, logic restructuring, input ordering. Glitching in static CMOS networks.

**Module 2**: **Dynamic & Leakage power reduction technique**

Dynamic Power reduction technique - Balanced delay paths to reduce glitching. Supply voltage reduction, power versus voltage, delay versus voltage. Clock gating. Multi-supply design: multiple VDD considerations, optimum numbers of supplies, dual-supply inside a logic block, level shifters, distributing multiple supply voltage: conventional and shared-well.

Dynamic power management vs. Dynamic voltage and frequency scaling. Choosing a frequency in DVFS. Total system energy variation in DVFS.

Leakage Power reduction techniques - Leakage power reduction techniques: multiple threshold, transistor stacking, input vector control, sleep transistor, variable threshold technique. Multiple threshold technique, dual threshold CMOS, using multiple thresholds. Transistor stacking self-reverse biasing, leakage control stacking. Input vector control: influence on subthreshold, gate, BTBT and total leakage.

**Module 3**: **Power Estimation, Synthesis for Low Power, Leakage reduction techniques**

Power Estimation – modeling of signals, probabilistic technique for signal activity estimation, statistical techniques, estimation of glitching power, power dissipation in Domino CMOS, power estimation in circuit level, high level power estimation, and estimation of maximum power.

Synthesis for low power - behavioral level transform, logic level optimization for low power, circuit level.

Leakage Reduction techniques - Sleep transistor technique: multi-threshold CMOS (MTCMOS), boosted-gate MOS (BGMOS), sizing of the sleep transistor, super cut-off CMOS (SCCMOS), zigzag super cut-off CMOS (ZSCCMOS).Variable threshold technique: variable threshold CMOS (VTCMOS), VTCMOS versus MTCMOS, dynamic Vth scaling (DVTS), dynamic threshold CMOS (DTMOS), double gate dynamic threshold (DGDT) SOI CMOS.

**Module 4**: **Low Power Logic Styles**

Advantages and disadvantages of static CMOS. Low-power logic styles: Pass-Transistor Logic (PTL), Complementary Pass-Transistor Logic (CPL), Pseudo-NMOS Logic, Dynamic Logic, Domino Logic, Adiabatic Logic. Pass-Transistor Logic. Ways to reduce leakage in PTL. Level restoration. CPL: Complementary Pass-Transistor Logic. Pseudo-NMOS Logic. Negative aspects of pseudo-NMOS. Dynamic logic. Characteristics of dynamic CMOS. Logic activity. Charge leakage. Problems with dynamic CMOS. Domino Logic. Selecting a logic style. Adiabatic Logic. Power saving and energy recovery. Charging with constant current, charge in N steps. Adiabatic dynamic CMOS inverter Quasi-Adiabatic Logic. Technology distribution. Power and area analysis.

**References:**


1. Gary Yeap " Practical Low Power Digital VLSI Design", Kluwer Academic.
2. Anantha P Chandrakaran, Robert W Broderson, “ Low Power Digital CMOS Design”, Kluwer Academic.
3. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", Wiley India.
4. C. Piguet. “Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools”. CRC. 2005.
5. James B Kuo, Jea-Hong-Lou, “Low Voltage CMOS VLSI Circuits”, Wiley Interscience.
6. Abdellatif Bellaouar, Mohammed I Elmasry, “ Low Power Digital VLSI Design Circuits and Systems”, Kluwer Academic.

7. Kaif Seng Yeo, Kaushik Roy, “Low Voltage Low Power VLSI Subsystems”, Tata McGraw Hill.

**MEC VE 105 - 4 SEMICONDUCTOR MEMORIES**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module I RANDOM ACCESS MEMORY TECHNOLOGIES**

Static Random Access Memories (SRAMS): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies- Silicon On Insulator (SOl) Technology- Application Specific SRAMs.
Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures- BiCMOS DRAMs-Soft Error Failures in DRAMs- Application Specific DRAMs.

**Module II NONVOLATILE MEMORIES**

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-EPROMs -Floating-Gate EPROM Cell

**Module III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE**

RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing- Nonvolatile Memory.Modeling and Testing—Application Specific Memory Testing

**Module IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability, Modeling and Failure Rate Prediction- RAM Fault Modeling, Electrical Testing, Peusdo Random Testing- Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-Application Specific Memory Testing.

**References:**

1. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing, and Reliability: Wiley- IEEE Press, 2002.

2 . Ashok K. Sharma, “Semiconductor Memories, Two-Volume Set”, Wiley-IEEE Press, 2003.
3. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing, & Reliability”, Prentice Hall of India, 1997.
4. Brent Keeth, R. Jacob Baker, DRAM Circuit Design: A Tutorial, Wiley-IEEE Press, 2000.
5. Betty Prince, High Performance Memories: New Architecture DRAMs and SRAMs - Evolution & Function, Wiley, 1999.

**MEC VE 106 - 1** **PROCESSOR ARCHITECTURE AND PARALLEL PROCESSING**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1**:

Basic pipelining and Simple RISC Processors: RISC Processors, ISA, examples, basic processor structure, basic pipelining, hazards and solutions, RISC processors-Early Scalar, Sun microSPARC-II, MIPS.

**Module 2**:

Dataflow Processors : Datafow verses Control flow, Pure Dataflow, Augmenting Dataflow with Control flow. CISC Processors: Overview, Out-of-order execution, Dynamic scheduling, examples.

**Module 3:**

Multiple- Issue processors :Overview, I- cache access and Instruction Fetch, Dynamic branch prediction and control speculation,, Decode, Rename, issue and dispatch, Execution stages, Finalizing pipelined execution, Principles of VLIW processors – TI TMS320C6x VLIW processors architecture.

**Module 4:**

Future processors to use Fine-Grain Parallelism, Future processors to use Coarse-Grain Parallelism, Processor in memory, Reconfigurable computing.

**References:**


1. Processor Architecture From Dataflow to Superscalar and Beyond By Jurij Silc, Borut Robic, Theo Ungerer, Springer.
2. Digital Signal Processing Implementation using the TMS320C6000 DSP Platform, Naim Dahnoun, Prentice Hall
3. Jurij Silc, Borut Robic, Theo Ungerer :“Beyond dataflow”, J. Computing and Information Technology, 8(2):89-101,2000

**MEC VE 106 - 2** **MODELING AND SIMULATION OF ELECTRONIC SYSTEM**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1**

Foundations : Axioms of arithmetic, proof by contradiction, mathematical induction, figurate numbers, binomial coefficients, Fibonacci numbers, division algorithm, radix representation of a number.

Divisibility : Divisors, greatest common divisor, least common multiple, Euclid's algorithm, prime factorization, relatively prime numbers, linear Diophantine equations, number and sum of divisors functions, perfect numbers, Mersenne primes,Fermat primes.

**Module 2**

Linear congruences: congruence relations, congruence arithmetic,complete residue systems, reduced residue systems, Euler's phi function, linear congruences, Chinese remainder theorem. Polynomial congruences : Polynomial factor theorem,Lagrange's theorem, quadratic residues, quadratic congruences, Wilson's theorem, Euler's criterion.

**Module 3**

Exponential congruences : Order of an integer modulo n, Fermat's and Euler's theorems, roots of unity, primitive roots, indices. Continued fraction algorithm, Pythagorean triples, four-squares theorem, Fermat's last theorem

**Module 4**

Introduction-directed and undirected graphs-varieties of graphs-the Königsberg bridge problem-traveling salesman problem-walks, paths and circuits-Euler graphs-Hamiltonian paths and circuits-Trees- panning tree-rooted tree-binary tree -representation of algebraic Structure of binary trees-counting trees-

Fundamental circuits-cut sets and cut vertices- connectivity and separability Planar graphs- Kuratowski's two graphs-dual graphs- matrix representation of graphs-incidence matrix-circuit matrix-cut set matrix-path matrix-colourability-chromatic number-matchings- coverings and independence-the four colour problem- directed graphs-digraphs-digraphs and matrices-tournaments

**References:**


1. Leveque, William, “Elementary Number Theory”, Dover Publications, Inc., NY, 1990
2. Neal Koblitz, “A Course in Number Theory and Cryptography”, 2nd Edition, Springer
3. Gross.JL and Yellen. “Graph Theory and its Applications” J CRC Press LLC, 1998
4. Diestel.R, “Graph Theory” Springer-Verlag 1997
5. West.DB, “Introduction to Graph Theory” Prentice Hall 1996

**MEC VE 106 - 3** **SYSTEM DESIGN USING ARM**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1:**

**General system design:** Embedded Computing : Introduction, Complex Systems and Microprocessor, The Embedded System Design Process, Formalisms for System Design, Design Examples.

**ARM Introduction:** Introduction to processor design-architecture and organization, Abstraction in hardware design, Instruction set design, Processor design trade offs, RISC. Overview of ARM architecture – Architecture inheritance, Programmer`s model, Development tools.

**Module 2: ARM Instruction Set:**

ARM assembly language programming, ARM organization and implementation, ARM instruction set (exceptions,conditional execution,branching instructions,multiply instructions,coprocessor instructions).

**Module 3:**

**Architectural support for high level languages**-Data types, Floating point data types,Conditional statements, Loops, Use of memory, Run-time environment

**Thumb instruction set**-Thumb bit, Thumb programmer`s model,Thumb branch instructions,Thumb software interrupt instructions

**Architectural support for system development**- ARM memory interface, AMBA, ARM reference peripheral specifications, h/w system prototyping tools, ARMulator, JTAG, ARM debug architecture, Embedded trace, signal processing support, ARM processor cores.

**Module 4:**

**Memory heirarachy**-Memory size and speed,On-chip memory, Caches, Memory management.

**Architectural support for OS-**Introduction, ARM system control coprocessor, ARM MMU architecture, Context switching

**Embedded ARM applications**-ARM7500 and ARM 7500FE & The SA-1100 **AMULET asynchronous ARM processors**-Self-timed design & AMULET1.

**References:**


1. ARM System-on-chip architecture, Steve Furber, Pearson Education
2. Computers as Components-principles of Embedded computer system design, Wayne Wolf, Elseveir
3. ARM System Developer`s Guide ,Andrew N Sloss, Dominic Symes, Chris Wright, Elseveir
4. An Embedded Software Primer, David E. Simon, Pearson Education.

**MEC VE 106 - 4 EMBEDDED NETWORKS & CONTROLLERS**

| L | T | P | C |
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**Module 1: Embedded Networking Requirements**

Network for Embedded Systems – I2C – CAN Bus – Blue tooth – SPI – USB – Ethernet protocol – TCP/IP Protocol – Internet connectivity over an Ethernet connection - Wireless Zig Bee standard.

**Module 2: Introduction to CAN + CAN Configuration**

CAN open standard - Object directory - Electronic Data Sheets & Device - Configuration files - Service Data Objectives - Network management CAN open messages - Device profile encoder. **-**CAN open configuration - Evaluating system requirements choosing devices and tools - Configuring single devices - Overall network configuration - Network simulation - Network Commissioning - Advanced features and testing.

**Module 3: CAN + MICRO CAN + Implementation**

CAN-Controller Area Network - Underlying Technology CAN Overview - Selecting a CAN Controller - CAN development tools

MICRO CAN- Implementing CAN open Communication layout and requirements - Comparison of implementation methods - Micro CAN open - CAN open source code - Conformance test - Entire design life cycle.

Implementation- Implementation issues - Physical layer - Data types - Object dictionary - Communication object identifiers - Emerging objects - Node states.

**Module 4: Microcontrollers in embedded networks**

PIC18FXX8 family, ARM® Cortex™-M3 microcontrollers

**References:**


1. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, "Embedded Networking with CAN and CAN open", Embedded System Academy 2005.
2. Wayne Wolf “Computers as Components: Priciples of Embedded Computing System Design”, Morgan Kaufman Publishers, 2008
3. PIC18FXX8 data sheets
4. ARM® Cortex™-M3 microcontrollers datasheets.

**MEC VE 107** **SEMINAR – I**

| L | T | P | C |
|---|---|---|---|
| 0 | 0 | 2 | 1 |

Each student shall present a seminar on any topic of interest related to the core / elective courses offered in the first semester of the M. Tech. programme. He / she shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.

**MEC VE 108** **VLSI DESIGN LAB**

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System simulation experiments based on the courses MEC VE 102, MEC VE 103 and the elective courses opted by the student in the first semester.

- HDL based digital design/simulation
- CMOS circuit design/simulation & layout design/simulation

| MEC VE 201 | ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS | L | T | P | C |
|---|---|---|---|---|---|
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**Module 1: MOS transistors**

MOS I/V characteristics – Second order effects - MOS modeling in linear, saturation and cutoff - high frequency equivalent circuit – Single stage amplifiers – common source stage – source follower – common gate stage – cascode and folded cascode stage

**Module 2:**

Differential amplifiers – basic differential pair – common mode response - Basic current mirrors – Cascode current mirrors – Active current mirrors

**Module 3:**

Frequency response – High frequency modeling - common source stage - source followers - common gate stage - cascode stage - differential pair – CMOS operational amplifiers – one-stage OPAMP – two-stage OPAMP – Need for compensation in OPAMPs – Dominant pole compensation – Pole-zero compensation

**Module 4:**

Statistical characteristics of noise - Noise spectrum and amplitude distribution - Correlated and uncorrelated sources - Thermal, Flicker and shot noise - Noise in amplifiers - Equivalent input noise generators - Noise calculation.

**References:**


1. Behzad Razavi, 'Design of Analog CMOS Integrated Circuit' Tata-Mc GrawHill, 2008
2. Gray, Hurst, Lewis, and Meyer, "Analysis and Design of Analog Integrated Circuits", 5th edition by, John Wiley and Sons, 2009
3. Philip Allen & Douglas Holberg, ' CMOS Analog Circuit Design', Oxford University Press, 2009
4. R. Gregorian, G.C. Temes, "Analog MOS ICs for Signal Processing", Wiley 2004.

**MEC VE 202 ADVANCED EMBEDDED SYSTEM DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module 1: State machine and concurrent process models**

Introduction Models vs. languages, A basic state machine model: finite-state machines (FSM), Finite-state machines with datapath model: FSMD.Using state machines, Hierarchical/Concurrent state machine model (HCFSM) and the Statecharts language, Program-state machine model (PSM), the role of an appropriate model and language, Concurrent process mode: Concurrent processes, Communication among processes, Synchronization among processes, Implementation Dataflow model, Real-time systems.

**Module 2: Advanced processors/Controllers ( ARM & DSPIC)**

Overview of ARM architecture, ARM organization and implementation

DSPIC architecture

**Module 3: Device Drivers & Interrupt servicing mechanisms**

Device drivers, Parallel port device drivers in a system, Serial port device drivers in a system, device drivers for internals,Interrupt sevicing mechanism,context and the periods for context-switching,deadline and interrupt latency

**Module 4: Embedded Software development tools**

Host and target machines, Linker/locator for embedded software, Getting embedded software into the target systems, debugging techniques, testing on your host machine, instruction set simulators, The assert macro.

**References:**


1. Frank Vahid ,Tony Givargis-Embedded System Design- Wiley Student Edition, India.
2. Raj Kamal "Embedded Systems – Architecture, Programming and Design", Tata McGraw Hill, 2nd Edition, 2008 ARM System-on-chip architecture, Steve Furber, Pearson Education
3. David E. Simon –A Embedded Software Primer – Pearson Education Inc.
4. DSPIC data sheets.

**MEC VE 203** **VLSI SYSTEM DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module 1**

Introduction to CAD Tools - Full custom design flow - specification to GDS-II - Types of standard cell elements, design of standard cell library, Study and implementation of standard cell library element.

**Module 2**

Semi-custom design flow – from specification to GDS II (Logic synthesis – Static Timing Analysis – System partitioning - floor planning – placement – global routing - detailed routing - circuit extraction – DRC – LVS).

**Module 3**

VLSI system components circuits-Multiplexers, decoders, Priority encoders, shift registers. Arithmetic circuits- ripple carry adders, carry look ahead adders, high-speed adders, Multipliers.

**Module 4**

System-on-Chip – Moving to SoC, Overview of SoC design process, Integrating platforms and SoC design, Introduction to Network-on-Chip.

**References:**


1. Introduction to VLSI Circuits and Systems, John P. Uyemura, John Wiley & Sons, Inc 2002.
2. Sung Mo Kang and Yusuf Lebelci, "CMOS Digital integrated Circuits Analysis and Design", Tata McGraw- Hill , New Delhi, 2003.
3. Jan M Rabaey and Anantha Chandrakasan, " Digital integrated Circuits- A Design Perspective" ,Prentice Hall, Second Edition, 2002.
4. Henry Chang, Larry Cooke, Merrill Hunt, Grant Martin, Andrew McNelly, Lee Todd, "Surviving the SOC Revolution A Guide to Platfrom – Based design", Kluwer Academic Publications 1999.

5. Neil H E Weste, David Harris and Ayan Banerjee," CMOS VLSI Design- A circuit System Perspective", Pearson Education, 2004.

6. Lin, Youn-Long Steve Ed. "Essential issues in SOC design : designing complex systems-on-chip".

**MEC VE 204 REAL TIME OPERATING SYSTEMS**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

**Module 1: Introduction to Embedded System and Real Time Operating system**

Basics of developing for embedded systems, Embedded System Initialization, Features of Operating Systems, Introduction to real time operating systems.

**Module 2: Kernel Scheduling and Data structures**

Tasks, Commonly Used Approaches to Real-Time Scheduling, Semaphores, Message queues, Pipes, Event registers, Signals, Condition Variables.

**Module 3: Dealing RTOS design issues**

Exceptions and Interrupts, Timer and Timer Services, I/O Subsystem, Memory Management.

**Module 4: RTOS porting on Embedded System**

Features of Vx Works.

Porting an Operating System like Micro OS or RT Linux on An Embedded Platform.

**References:**


1. Real-Time Concepts for Embedded Systems By Qing Li, Caroline Yao, CMP Books.
2. Real-Time Systems, by Jane W. S. Liu.
3. Real- Time Systems Design and Analysis by Philip A. Laplante, Wiley Student Edition.
4. Real Time Systems, by Krishna and Shin , Mc Graw Hill.
5. Shibu K V "Introduction to Embedded Systems", Tata McGraw Hill, 2010.

**MEC VE 205 - 1** **DSP SYSTEM DESIGN**

| L | T | P | C |
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**Module 1**

Introduction to a popular DSP from Texas Instruments TMS320C6XXX– CPU Architecture (VLIW) - CPU Data Paths and Control - Timers - Internal Data/ Program Memory - External Memory Interface ,Difference between fixed and floating point processors.

**Module 2**

DSP devices beyond the core, TI C6xxx EVM memory configuration, wait state generator, DMA, Hardware interfacing and I/O control, System management and control.

**Module 3**

Programming - Linear and Circular Addressing Modes, Assembly code format, Types of Instructions, Assembler directives Code Composer Studio - Code Generation Tools (Compiler, Assembler, Linker) - Code Composer Studio Debug Tools – Simulator.

**Module 4**

Adaptive filtering Introduction to adaptive filters, adaptive filter structures and algorithms, Properties of adaptive filters, Applications, Adaptive filtering in C using floating-point processors.

**References:**


1. Naim Dahnoun, Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1st Edition, 2000.
2. Rulph Chassaing, "DSP Applications using 'C' and the TMS320C6X DSK", 1st Edition, 2002.
3. Andrew Bateman, Iain Paterson-Stephens, The DSP Handbook – Algorithms, Applications and Design Techniques, Pearson Education.
4. Sen M Kuo, Woon- Seng S Gan, Digital Signal Processors Architectures, Implementations and Applications, Pearson Education.

**MEC VE 205 -2 MEMS & MICRO SYSTEM TECHNOLOGY**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1:**

History of MicroElectroMechanical Systems (MEMS), market for MEMS, MEMS Materials: Silicon and other materials , mechanical properties of materials- elasticity, stress and strain, Beams & Structures –cantilevers and bridges, point load & uniform loading, torsional, dynamic system; Piezoelectric & piezoresistive materials.

**Module 2:**

MEMS fabrication processes: Review of IC fabrication process, Micromachining: Bulk micromachining (dry and wet etching), Surface micromachining (deposition, evaporation, sputtering, epitaxial growth), Deep RIE, Advanced Lithography, LIGA process; Multi User MEMS Process.

**Module 3:**

MEMS Devices & Packaging: MEMS Sensors and Actuators (Electrostatic, Electromagnetic, Thermal and Piezo), Bio-MEMS, Optical MEMS, Micro-fluidics MEMS; MEMS packaging issues, die-level packaging, micro assembled caps & sealing.

**Module4:**

Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD), Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT), Air bag system, Micromotors, Scanning Probe Microscopy.

**References:**


1. Foundation of MEMS, Second Edition 2011 – Chang Liu, Pearson.
2. Gregory T A, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill, 1998.
3. Microsystem Design – by Stephen D. Senturia, Publishers: Kluwer Academic / Springer, 2nd Edition (2005), ISBN: 0792372468
4. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 2002.

5. Nadim Maluf, An introduction to Microelectromechanical system design, Artech House, 2000
6. Mohamed Gad-el-Hak, Editor, The MEMS Handbook, CRC Press, Baco Raton, 2002.

**MEC VE 205 - 3** **VLSI SIGNAL PROCESSING**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1:**

Representation of DSP algorithms.

Iteration Bound: Loop Bound, Iteration Bound, Algorithms, Iteration Bound for multirate data flow graphs.

Pipelining and Parallel Processing: Introduction, pipelining of FIR filters, parallel processing.

**Module 2: Timing Techniques**

Retiming: introduction, properties, system inequalities, retiming techniques

Unfolding: Introduction, algorithm, properties, critical path, sample period reduction

Folding: Introduction, Transformation, register minimization

**Module 3: DSP Architectures**

Systolic architecture design: Introduction, Design Methodologies, FIR systolic array, matrix matrix multiplication.

Fast convolution: Cook Toom, Winograd, Iterated convolution.

Parallel FIR filters: Fast FIR, parallel architecture for rank order filters.

**Module 4: Pipelining of recursive filters**

Introduction, pipeline interleaving, parallel processing in IIR filters,Scaling and round off noise computation, Bit level arithmetic architecture, parallel multipliers, bit serial multipliers, Canonic Singed digit arithmetic, distributed arithmetic.

**References:**


1. Keshab V Parhi, VLSI Digital Signal Processing, Willey India.
2. Peter Pirsch, Architecture for Digital Signal Processing, Wiley.
3. Magdy A Bayoumi, VLSI design methodologies for DSP architecture.

**MEC VE 205 - 4 HARDWARE SOFTWARE CO-DESIGN**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1**

Specification of embedded systems- Why Co-design? –Comparison of co-design approaches-MoCs: State oriented, Activity oriented, Structure oriented, Data oriented and Heterogeneous- Software CFSMs-Processor Characterization.

**Module 2**

HW/SW Partitioning Methodologies-principle of hardware/software mapping-Real time scheduling-Design specification and constraints on embedded systems- trade offs – Partitioning granularity-Kernigan-Lin Algorithm- Extended Partitioning- Binary Partitioning: GCLP algorithm.

**Module 3**

Co-synthesis & Estimation –Software synthesis –Hardware Synthesis –Interface Synthesis- Co-synthesis Approaches: Vulcan, Cosyma, Cosmos, Polis and COOL-estimation: Hardware area, execution timing and power: Software memory and execution timing.

**Module 4**

Co-simulation and Co-verification- principles of co-simulation-abstract level: detailed level co-simulation as partition support-cosimulation using Ptolemy approach.

**References:**


1. Felice Balarin, Massimiliano Chiodo Paolo Giusto, Harry Hsieh, Attila Jurecska, Luciano Lavagno, Claudio Passerone, Alberto Sangiovanni- Vincentelli, Ellen Sentovich, Kei Suzuki, Bassamssam Tavvara, “Hardware-software co-design of embedded system: POLIS Approach”, Springer, 2004.
2. Raf Niemann, “Hardware/ Software Co-design for Data Flow Dominated Embedded Systems”, Spring, 1998.
3. Peter Marwedel, “Embedded System Design”, Springer, 2009.
4. Russlell John Rickford, Bernd kleinjohann, “Design and Analysis of Distributed Embedded Systems”, Springer, 2002.

**MEC VE 206 - 1 ANALOG & MIXED VLSI CIRCUITS**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1:**

Depletion region of a PN junction-Large signal model of bipolar transistors-small signal model of biplolar transistor-short channel effects in MOS transistors-weak inversion in MOS transistors-substrate current flow in MOS transistor.

**Module 2:**

Analysis of difference amplifiers with active load using BJT and FET- Supply and Temperature independent biasing techniques-voltage references. Output Stages-Emitter follower-source follower and push pull output stages.

**Module 3:**

Configuration for Linear IC Current sources-current mirrors- designs-difference amplifiers with active load- biasing techniques-voltage reference-CMOS voltage reference-MOS power amplifier and analog switches-Analog multiplier and PLL-VCO-Closed loop analysis of PLL

**Module 4:**

MOS switched Capacitor filters-Design-switched capacitor filter-CMOS switched capacitor filters-MOS active RC filters. Mixed signal Design: Delta sigma modulators

**References:**


1. Phillip E Allen and Douglas R Holberg “CMOS Analog Circuit Design”, Oxford University Press, USA, 2002.
2. Behzad Razavi, “Analysis and Design of CMOS integrated Circuits”, Tata Mc Graw Hill, 2008.
3. Gray, Meyer, Lewis Hurst “Analysis and Design of Analog IC”, Wiley International 4th Edition, 2009.
4. Nandita Dasgupat, Amitava Dasgupta “Semiconductor Devices: Modelling and Technology”, Prentice Hall of India, 2007

**MEC VE 206 - 2** **TESTING OF VLSI CIRCUITS**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module1:**

Introduction-VLSI testing process and Test Equipment-Test Economics and Product Quality- why fault modeling-Fault Modeling-Logic and Fault Simulation-glossary of Faults-single stuck-at-faults-functional equivalence-bridging faults.

**Module 2:**

Logic simulation-modeling single states-algorithm for true value simulation-serial and parallel fault simulation-Testability Measures-Combinational Circuit Test Generation-Sequential Circuit Test Generation.

**Module 3:**

Design for testability – Digital DFT and Scan design, Built-in Self test- random logic BIST and memory logic BIST, Boundary Scan standard.

**Module 4:**

Memory Test-Analog and Mixed signal Test-delay test-IDDQ Test. DFT Fundamentals-ATPQ Fundamental-Scan Architecture and Technique. System Test- Embedded Core Test-Future Testing.

**References:**


1. Viswani D Agarwal and Michael L Bushnell, “Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits”, Springer, 2000.

2. Alfred L Cronch, “Design for Test for Digital IC’s and Embedded Core system”, Prentice Hall, 1999.

3. Niraj Jha and Sanjeep K Gupta, “Testing of Digital Systems”, Cambridge University Press, 2003.

4. M. Abramovici, M A Breuer and A D Friedman, “Digital systems Testing and Testable Design”, IEEE Press, 1994.

**MEC VE 206 - 3** **CAD FOR VLSI**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module 1:**

Introduction to VLSI Design methodologies and abstraction levels – Introduction to VLSI design automation tools – Introduction to algorithmic graph theory – Computational complexity – Tractable and Intractable problems - Combinational optimization.

**Module 2:**

Hardware modeling - High level synthesis – Internal representation - allocation – assignment – scheduling – scheduling algorithms – Integer linear programming – Hueristic: list scheduling & force-directed scheduling.

**Module 3:**

Layout Compaction – design rules – problem formulation – algorithms for constraint graph compaction – placement & partitioning algorithms.

**Module 4:**

Floor planning concepts – shape functions and floorplan sizing – types of routing problems.

Simulation – gate level modeling and simulation – switch level modeling and simulation.

**References:**


1. Sabih. H. Gerez, "Algorithm for VLSI Design Automation Theory and Practice", John Willey & Sons Ltd., 2004
2. Naveed Sherwani "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International edition, 2005.
3. Giovanni De Micheli "Synthesis and Optimization of Digital Circuits", 1st Edition Mc Graw Hill, 1994.
4. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education Asia, 2009.
5. H Yosuff and S M Sait "VLSI Physical Design Automation Theory and Practice", Mc Graw Hill Pub. , 1995.

**MEC VE 206 - 4** **RECONFIGURABLE COMPUTING**

| L | T | P | C |
|---|---|---|---|
| 3 | 0 | 0 | 3 |

**Module I**

Introduction to Adaptive/Reconfigurable Computing – Computing Requirements, area, and VLSI scaling – Instructions – Introduction to FPGA – Custom Computing Machine Overview – Comparing Computing Machines

**Module II**

FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms - Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures – Bit Serial.

**Module III**

Adaptive Network Architectures – Static and Dynamic network – Routing/embedding Rearrangeable networks – Reconfigurable bus – Dynamic reconfiguration issues – Reconfiguration delay – Partial reconfiguration – OS support – Reconfigurable Operating Systems – Device and task models – Multitasking and runtime systems – Dynamically Reconfigurable Adaptive Viterbi Decoder.

**Module IV**

Reconfigurable Computing Architectures – Reconfigurable coprocessor based architectures – Compiler technology for coprocessor based architectures – Mapping/scheduling algorithm – Reconfigurable pipelines – Reconfigurable memories & caches – Reconfigurable Computing Applications**,** reconfigurability using Virtex T series**.**

**References:**


1. John V.Oldfield and Richard C. Dorf, "Field Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems", John Wiley & Sons, Inc., 1995.
2. Configware Reiner W. Hartenstein, Viktor K. Prasanna (Eds.): "Reconfigurable Architectures: High Performance", IT press Verlag, 1997.
3. Wayne Wolf, "FPGA- based System Design", Prentice Hall, 2004.
4. R.Vaidynathan and J. I., Trahan, "Dynamic Reconfiguration: Architectures and Algorithms", Khuwer Academic/Plenum Publishers, New York, 2004.l

**MEC VE 207** **SEMINAR – II**

| L | T | P | C |
|---|---|---|---|
| 0 | 0 | 2 | 1 |

Each student shall present a seminar on any topic of interest related to the core / elective courses offered in the second semester of the M. Tech. programme. He / she shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.

**MEC VE 208** **EMBEDDED SYSTEM LAB**

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System simulation experiments based on the courses MEC VE 104, MEC VE 202, MEC VE 204 and the elective courses opted by the student in the second semester.

- Embedded System IDE based simulations
- Real Time applications development

**MEC VE 301 INDUSTRIAL TRAINING AND MINI PROJECT**

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The student shall undergo

i) An Industrial Training of 12 weeks duration in an industry / company / institution approved by the institute under the guidance of a staff member in the concerned field.

**OR**

ii) Industrial Training of 1 month duration and Mini Project of 2 months duration in an industry / company / institution approved by the institute under the guidance of a staff member in the concerned field. At the end of the training he / she have to submit a report on the work being carried out.

**MEC VE 302 MASTER'S THESIS PHASE - I**

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The thesis (Phase - I) shall consist of research work done by the candidate or a comprehensive and critical review of any recent development in the subject or a detailed report of project work consisting of experimentation / numerical work, design and or development work that the candidate has executed.

In Phase - I of the thesis, it is expected that the student should decide a topic of thesis, which is useful in the field or practical life. It is expected that students should refer national & international journals and proceedings of national & international seminars. Emphasis should be given to the introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work / experimentation carried out on the thesis topic. Student should submit two copies of the Phase - I thesis report covering the content discussed above and highlighting the features of work to be carried out in Phase – II of the thesis. Student should follow standard practice of thesis writing. The candidate will deliver a talk on the topic and the assessment will be made on the basis of the work and talks there on by a panel of internal examiners one of which will be the internal guide. These examiners should give suggestions in writing to the student to be incorporated in the Phase – II of the thesis.

**MEC VE 401** **MASTER'S THESIS**

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In the fourth semester, the student has to continue the thesis work and after successfully finishing the work, he / she have to submit a detailed thesis report. The work carried out should lead to a publication in a National / International Conference. They should have submitted the paper before M. Tech. evaluation and specific weightage should be given to accepted papers in reputed conferences.

**MEC VE 402** **MASTER'S COMPREHENSIVE VIVA**

A comprehensive viva-voce examination will be conducted at the end of the fourth semester by an internal examiner and external examiners appointed by the university to assess the candidate's overall knowledge in the respective field of specialization.